CLAIMS

1. A probe for wafer-level testing and/or burn-in of electronic components, comprising:

a mosaic comprising a plurality of probe chips;

a membrane onto which said mosaic of probe chips is affixed; and

a ring from which said membrane is suspended, and by which said membrane is optionally held in tension, said ring being made of a material that has a thermal coefficient of expansion (TCE) substantially matching that of said wafer.

2. The probe Claim of 1, wherein said electronic components comprise any of: a plurality of semiconductor devices; a plurality of surface acoustic wave devices; a plurality of light emitting devices; a plurality of liquid crystal display devices; and a plurality of MEMS devices.

3. The probe of Claim 1, wherein each of said probe chips comprises a first surface and an opposite surface, and further comprises a plurality of spring contacts formed on both surfaces thereof; and

wherein said probe chip optionally comprises multi-layer metallization.

4. The probe of Claim 3, wherein at least one spring contact on said first probe chip surface is electrically connected to at least one spring contact on said opposite probe chip surface;

wherein at least one spring contact on said first probe chip surface is optionally electrically connected to at least one spring contact on said opposite probe chip surface through an electrically conducting via.

5. The probe of Claim 3, said membrane further comprising apertures formed therethrough to allow spring contacts on one side of said membrane to protrude through said membrane.

6. The probe of Claim 1, further comprising a printing wiring board, having a surface profile with recesses matching the pattern of the membrane.

7. The probe of Claim 1, wherein said mosaic comprises a low-count mosaic comprised of a small number of probe chips;

wherein said probe chips have a substantially same TCE as a test wafer.

8. The probe of Claim 1, wherein each said probe chip is at least peripherally attached to said membrane.

9. The probe of Claim 1, wherein said mosaic comprises a high-count mosaic comprised of a large number of probe chips which can have a slight TCE difference from that of a test wafer.

10. The probe of Claim 1, wherein each said probe chip is center attached to said membrane.

11. The probe of Claim 1, wherein said ring is comprised of any of molybdenum, silicon, and glass-ceramic.

12. The probe of Claim 1, wherein said membrane is comprised of any of a flexible film, flexible polymer film, and polyimide film.

13. The probe of Claim 1, wherein said mosaic of probe chips is affixed to said membrane with an adhesive that is applied to regions between a surface of each probe chip and said membrane.

14. The probe of Claim 13, wherein said adhesive is applied in the center of each of said probe chips to hold said probe chips together.

15. The probe of Claim 1, wherein said membrane and said mosaic of probe chips are laminated.

16. The probe of Claim 1, wherein said mosaic of probe chips is affixed to said membrane with an adhesive that is applied to a periphery of each of said probe chips.

17. The probe of Claim 14, wherein one or more adhesive dots dispensed over small apertures in said membrane are used to secure said mosaic of probe chips to said membrane.

18. The probe of Claim 3, further comprising:

a printed wiring board; and

a plurality of land pads formed on a surface of said printed wiring board, wherein said land pads are arranged to complement spring contacts formed on a surface of a probe chip.

19. The probe of Claim 18, further comprising:

at least one recessed region defined in said printed wiring board that accommodates at least one projected region from the said surface of at least one probe chip;

wherein the said projected region optionally comprises either of layers of adhesive and membrane, or adhesive dots.

20. A probe apparatus, comprising:

a printed wiring board;

a plurality of land pads formed on a surface of said printed wiring board, wherein said land pads are arranged to complement spring contacts formed on a surface of at least one probe chip; and

at least one recessed region defined in said printed wiring board that accommodates at least one projected region from the said surface of at least one probe chip.

21. The Claim of 20, wherein the said projected region comprises either of layers of adhesive and membrane or adhesive dots.

22. A probe method for wafer-level testing and/or burn-in of electronic components, comprising in any sequence the steps of:

providing a mosaic comprising a plurality of probe chips;

affixing said mosaic of probe chips onto a membrane; and

suspending said membrane from a ring, said ring being made of a material that has a thermal coefficient of expansion (TCE) substantially matching that of said wafer.

23. The method of Claim 22, wherein a tensile stress is additionally applied to said membrane during ring attachment

24. The method of Claim 22, wherein each of said probe chips comprises a first surface and an opposite surface, and further comprises a plurality of spring contacts formed on both surfaces thereof.

25. The method of Claim 24, wherein at least one spring contact on said first probe chip surface is electrically connected to at least one spring contact on said opposite probe chip surface.

26. The method of Claim 24, further comprising the step of:

forming apertures through said membrane to allow spring contacts on one side of said membrane to protrude through said membrane.

27. The method of Claim 24, wherein said spring contacts are allowed to slide along a contacted surface during temperature excursions.

28. The method of Claim 22, wherein said mosaic comprises a low-count mosaic comprised of a small number of probe chips;

wherein said probe chips have a substantially same TCE as a test wafer.

29. The method of Claim 25, further comprising the step of:

peripherally attaching each of said probe chips to said membrane.

30. The method of Claim 22, wherein said mosaic comprises a high-count mosaic comprised of a large number of probe chips which can have a slight TCE difference from that of a test wafer.

31. The method of Claim 27, wherein at least one of said plurality of probe chips is center attached to said membrane.

32. The method of Claim 22, wherein said ring is comprised of any of molybdenum, silicon, and glass-ceramic.

33. The method of Claim 22, wherein said membrane is comprised of any of a polyimide film, a flexible film, and a flexible polymer film.

34. The method of Claim 22, further comprising the step of:

affixing said mosaic of probe chips to said membrane with an adhesive that is applied to regions between a surface of each probe chip and said membrane.

35. The method of Claim 31, further comprising the step of:

applying said adhesive along an outside and on an inside of each of said probe chips to hold said probe chips together.

36. The method of Claim 22, further comprising the step of:

laminating said membrane and said mosaic of probe chips.

37. The method of Claim 22, further comprising the step of:

affixing said mosaic of probe chips to said membrane with an adhesive that is applied to a periphery of each of said probe chips.

38. The method of Claim 37, further comprising the step of:

dispensing one or more adhesive dots over small apertures in said membrane to secure said mosaic of probe chips to said membrane.

39. The probe method of Claim 22, further comprising the step of:

providing a printed wiring board having land pads arranged to complement said spring contacts formed on said first or said other surface of said probe chips, said printed wiring board having at least one recessed region defined in said printed wiring board that accommodates at least one projected region from the said surface of at least one probe chip; and

wherein said projected region optionally comprises either of layers of adhesive and membrane or adhesive dots.

40. A probe method, comprising the steps of:

providing a printed wiring board;

providing a plurality of land pads formed on a surface of said printed wiring board, wherein said land pads are arranged to complement spring contacts formed on a surface of a probe chip; and

providing at least one recessed region defined in said printed wiring board that accommodates at least one projected region from the said surface of at least one probe chip.

41. The method Claim of 40, wherein the said projected region comprises either of layers of adhesive and membrane or adhesive dots.